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WHAT IS CLAIMED IS:

1. A memory circuit apparatus comprising:

a plurality of memory cells connected to a plurality of bit lines and word lines;

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an access circuit connected to the plurality of bit lines and word lines to select predetermined memory cells from the plurality of memory cells in response to an address signal;

a precharge circuit which precharges the bit lines connected to the memory cells selected by the access circuit at the time of a read mode;

a common source line connected to a plurality of selected memory cells selected by the access circuit;

a source line potential control circuit to connect the common source line to a ground node at a predetermined timing; and

a discharge circuit which discharges the bit lines connected to non-selected memory cells other than the selected memory cells.

- 2. The memory circuit apparatus according to claim 1, wherein the discharge circuit is connected to the bit lines connected to the non-selected memory cells, and includes a plurality of discharge transistors to fix these bit lines at a ground potential.
 - 3. The memory circuit apparatus according to claim 2, wherein the discharge circuit includes a

decoder circuit which receives the address signal and a discharge permission signal as inputs and which produces an on signal to be supplied to the discharge transistors.

- 5 4. The memory circuit apparatus according to claim 1, wherein one end of the bit line is connected to a precharge power supply via the access circuit and precharge circuit, and the other end of the bit line is connected to a ground node via the memory cell and the source line potential control circuit.
 - 5. The memory circuit apparatus according to claim 1, wherein the source line potential control circuit includes a switching device controlled to turn on/off by a source line potential control signal, and connects the source line to the ground potential, when the switching device turns on.
 - 6. The memory circuit apparatus according to claim 1, wherein the memory cell comprises a nonvolatile memory cell constituting E^2 PROM.

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- 7. The memory circuit apparatus according to claim 1, wherein the memory cell comprises a MOS transistor in which a source is selectively connected to a drain via a metal wiring, and constitutes a NOR type MROM.
- 25 8. The memory circuit apparatus according to claim 1, wherein the memory cell comprises a MOS transistor in which a source is selectively connected

to a drain via a metal wiring, and constitutes a NAND type MROM.

9. The memory circuit apparatus according to claim 1, wherein the access circuit includes a column decoder which selects a predetermined bit line by an input address signal, and the discharge circuit supplies an off signal to a discharge transistor connected to a predetermined bit line selected by the same input address signal as that of the column decoder.

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- 10. The memory circuit apparatus according to claim 9, wherein the discharge circuit includes a decode circuit which produces the same decoded output as that of the column decoder, and an inverter which reverses a polarity of the output of the decode circuit.
- 11. The memory circuit apparatus according to claim 1, wherein the plurality of memory cells are grouped/divided in a plurality of memory blocks, and the memory cells in each block are further grouped/divided into a plurality of words.